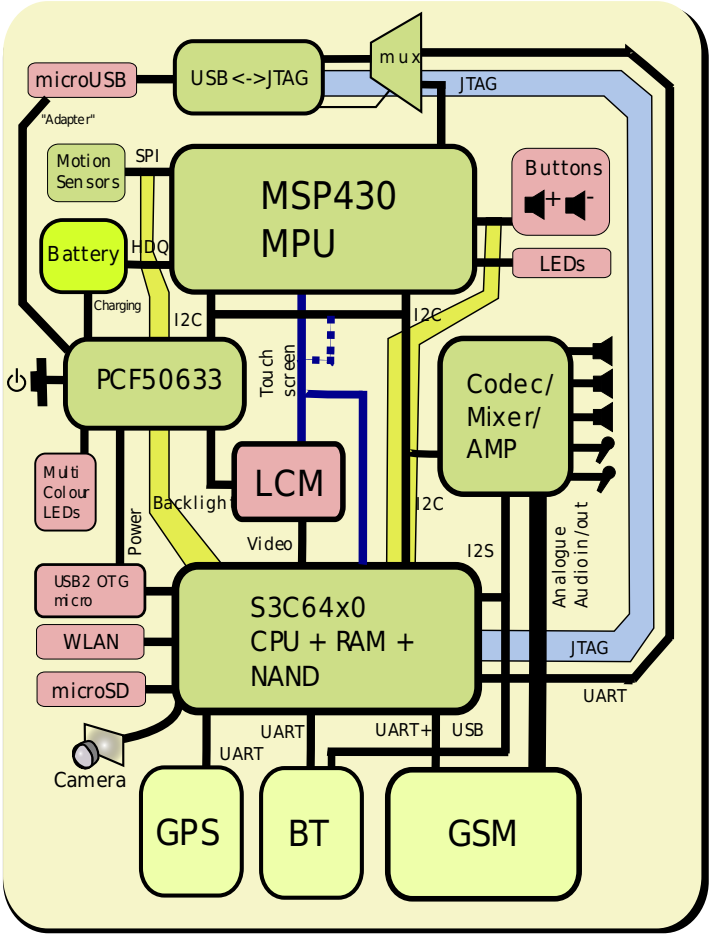
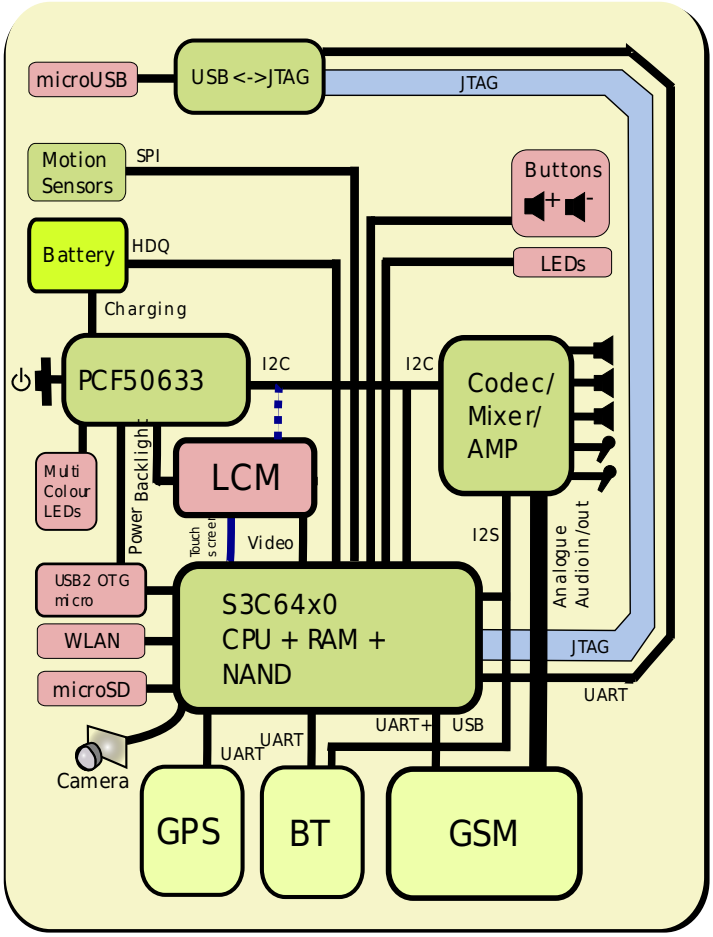
Preferred design, used on first prot type

2008 Core Arch proposal with MSP430 versio 5



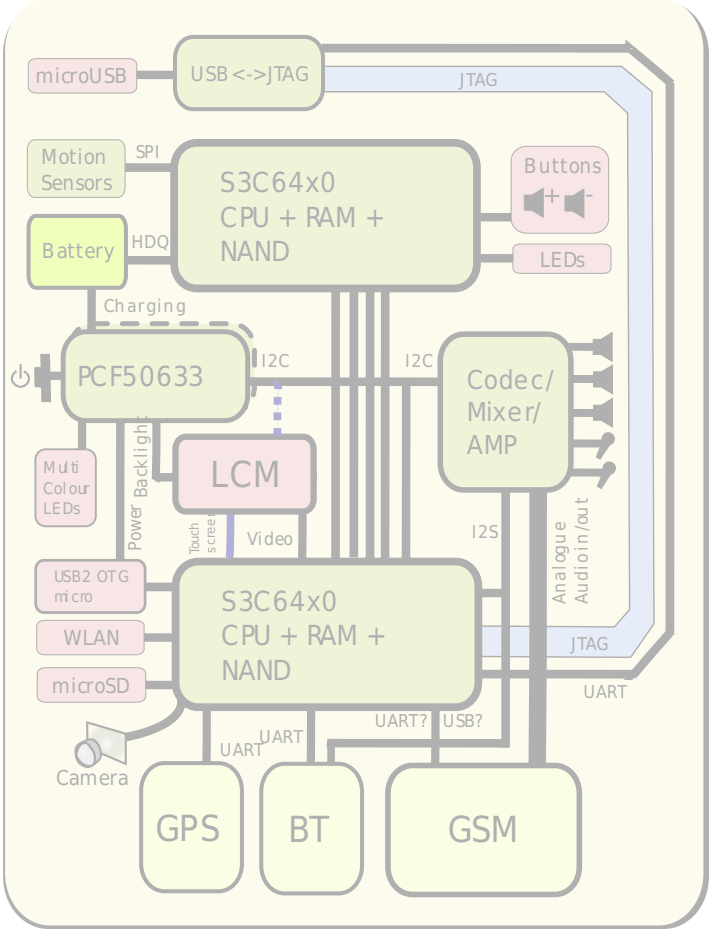
Possible cost optimization if PMU alows

2008 Core Arch proposal CPU ONLY version 2



Alternative we won't follow up for now

2008 Core Arch proposal TWO CPUs version 1



Comparison	MPU	no-MPU	2 x CPU
Smarts while CPU down	Some	None	Some
eg, flash LEDs during cal	Yes	No	Yes
Power management,	MPU	Linux	CPU-2
PMU handling,	MPU / Linux	Linux	CPU-2
charging modes,	MPU / Linux	Linux	CPU-2
battery status / HDQ	MPU	FIQ ISR	FIQ ISR CPU-2
Power management OK during boot	Yes	Unresponsive	Yes
Wake dead time			
seamless motion capture	Yes	No + Linux driver	Yes
seamless touchscreen capture	Yes (big MPU)	No + Linux driver	Yes
button lag covering	Some	No	Some
Production test assist			
get suspend current while cpu down	Yes	No	Yes
Need to create MPU firmwar	Yes	No	Yes / ARM9
Need to deal with power and charging	Some	All	Some
logic inside Linux / Bootloader	(logical USB)		(logical USB)
Wake CPU scheduling	MSP430 queue	6400 RTC	CPU-2
JTAG chain	2 deep	1 deep	2 deep
Power in standby (standby time)[1]	Longest	Shortest	Medium
PMU sequencing risk[2]	Low	Unsolved	Unsolved

MSP430 selection

9mm

64QFN 9mm

MSP430F417
$4.90/100

7.1mm

BGA 7.1mm

MSP430FG4618
$12.95/100

First prototype anyway

No MPU

$0
No lead time

[1] Assumes that CPU-2 Flash and DDR are turned off, running from only rom

[2] There is a concern the power sequencing and levels put out by PCF5 05 default may not be good for the CPU. MPU can come up first and let them exactly right since it will not depend on PMU sequencing itself